REMARKS

Applicant respectfully traverses and requests reconsideration.

Claims 3-5 stand rejected under 35 USC 112, second paragraph due to a lack of antecedent basis for the claimed limitation of "decoded video." Applicants have herein amended claims 3-5 to correct the noted informality, amended the element "active decoded video" to "active video." Moreover, Applicants submit the claimed limitation of "active video" maintain proper antecedent basis with respect to claim 1. As such, Applicants respectfully request reconsideration and withdrawal of the above-noted rejection.

Claims 1-2 stand rejected under 35 USC 102(e) as being anticipated by US Patent No. 5,694,150 ("Sigona"). Sigona teaches a graphical user interface system having an event-driven control program with a unified user input pointing event stream without distinction of source and a graphical user interface having a virtual display space. Sigona applies a multiple screen display driver (14 and 15) system (1) to provide a multi-user environment on displaced portions (4 and 12) of a large virtual image space, such as a single or multiple screens. The system provides each of a plurality of users, specific and uninterrupted control over a dedicated region or shared region of the virtual display space. Moreover, the system operates in two distinct modes, the first mode provides for the multiple users to operate independent of each other and in the second mode, the multiple users operate in cooperation.

Regarding claim 1, the present invention claims a method for displaying active video on a computer system. Sigona fails to disclose, *inter alia*, receiving a first frame of active video from a video source at a first video graphics adapter. Sigona teaches multiple display drivers which provide display of user input, which is not consistent with the claimed first frame of active video. Moreover, Sigona fails to disclose, *inter alia*, rendering at least a first portion of the first frame of video at the first VGA in response to a first control signal and rendering at least a second portion of the first frame of video at a second VGA in response to a second control signal. The Examiner supports the rejection with reference to FIG. 3, which illustrates multiple inputs (2 and 3) provided to the system (1) where two output signals (14 and 15) are generated and provided to multiple displays (4 and 12). Fig. 3 and accompanying discussion does not disclose, *inter alia*, at least a first portion of the first frame and/or a first control signal, at least a second portion of the

first frame and/or a second control signal. Moreover, the system of Sigona would not render a first portion of a first frame or a second portion of the same frame using two different VGA's, but rather would render the full frame and then sends the same output signal into either output signal 14 and 15 depending on which screen the output is to be displayed. As such, Applicants respectfully submit that Sigona fails to disclose the claimed limitations of claim 1. Applicants request reconsideration and withdrawal of the above-noted rejection. In the event the Examiner should maintain the rejection, Applicants expressly request a showing, including column and line numbers, of where the claimed limitations are expressly disclosed by Sigona.

Regarding claim 2, Applicants submit the position offered above with respect to claim 1. Furthermore, Applicants respectfully submit that Sigona fails to disclose wherein the first portion and the second portion are the same portion. The Examiner has referenced FIG. 3 in support of the rejection. Applicants assert confusion regarding where Sigona discloses a first frame of video, much less the further limitations of the video having a first portion and a second portion. As stated above, the system of Sigona (1) renders the full input signal, from either or both inputs depending on mode of operation, and then parses the signal to either display (14 or 15) or both which is inconsistent with claimed limitations of claim 2. As such, Applicants respectfully submit that Sigona fails to disclose the claimed limitations of claim 2. Applicants request reconsideration and withdrawal of the above-noted rejection. In the event the Examiner should maintain the rejection, Applicants expressly request a showing, including column and line numbers, of where the claimed limitations are expressly disclosed by Sigona.

Claims 14-16 and 18-19 stand rejected under 35 USC 102(e) as being anticipated by US Patent No. 5,374,940 (Corio). Corio teaches a system for operating multiple displays from a single computer without having to modify the computer hardware and the video boards may be resident within their usual expansion slots. The multiple video boards generate graphics images representing data in response to data signals and control signals. Each video board is used to generate a separate display. The video boards are connected to intercepting circuits to provide address, data, and control signals. The video boards process data into images and apply the images to be displayed on monitors, wherein either the first board or the second board is enabled to receive image data and provide an original or updated image to either the first monitor or the second monitor, respectively.

Regarding claim 14, Corio fails disclose, *inter alia*, monitoring the location of an active video window. Corio discloses, among other things, upon initialization, a first board enabled by a reset signal and the second board disabled. If an instruction to change the display of the first video board is received, the second video board is disabled and the first video board is enabled and updated. Otherwise the program looks for an instruction to change the display of the second video board. This is inconsistent with the claimed limitation of "monitoring the location of an active video window," as Corio is not concerned with the location of active video window, but rather only which video board is enabled/disabled. Moreover, Corio fails to disclose, *inter alia*, "storing the active video data at a first video memory." The Examiner sites to col. 4, lines 20-26 which disclose that the video board has a memory, but Applicants submit this is inconsistent with storing the active video data as Corio only accesses the video board when an image is to be displayed, not disclosing actually storing the active video data. Furthermore, Corio fails to disclose, *inter alia*, "sending the active video data from the first video memory to a second video memory when the location of the active video window is associated with the video memory" as the system of Corio is not designed to send active video data from the first video board to the second board, much less transmit video data from the memory within the first video board to the memory within the second video board. The video signals and enable/disable signals are provided from the CPU to either the first board or the second board and the first board and second board do not interact, therefore Corio would never have active video data sent from the memory of the first video board to the memory of the second video board. As such, Applicants respectfully request reconsideration and withdrawal of the above-noted rejection. In the event the Examiner should maintain the rejection, Applicants expressly request a showing, including column and line numbers, of where the claimed limitations are explicitly disclosed by Corio.

Regarding claim 15, Applicants resubmit the above-position regarding claim 14 and further assert the Corio fails to teach or suggest receiving at a first VGA a first frame of active video from a video source and displaying at least a first portion of the first frame of video at a second VGA in response to a second control signal. As discussed above, Corio either enables or disables each board, therefore Corio could not provide a frame of video to the first board and display via the second board. As such, Applicants respectfully request reconsideration and withdrawal of the above-noted rejection. In the event the Examiner should maintain the

rejection, Applicants expressly request a showing, including column and line numbers, of where the claimed limitations are explicitly disclosed by Corio.

Regarding claim 16 Applicants respectfully resubmit the position regarding claims 14 and 15. It is further submitted that claim 16 contains further limitations not disclosed by Corio, such as the video source being a video decoder. Corio teaches, *inter alia*, the video source being provided from the CPU, but fails to disclose a video decoder. Therefore, Applicants respectfully request reconsideration and withdrawal of the above-noted rejection. In the event the Examiner should maintain the rejection, Applicants expressly request a showing, including column and line numbers, of where the claimed limitations are explicitly disclosed by Corio.

Regarding claim 18 Applicants respectfully resubmit the position regarding claims 14, 15 and 16. It is further submitted that claim 18 contains further limitations not disclosed by Corio, such as the video source sending the first frame of data over a local bus. Corio teaches, *inter alia*, the video source being provided from the CPU, but succinctly discloses that CPU is not connected to the expansion slot housing the video boards using a local bus, see col. 3, lines 48-53. Therefore, Applicants respectfully request reconsideration and withdrawal of the above-noted rejection. In the event the Examiner should maintain the rejection, Applicants expressly request a showing, including column and line numbers, of where the claimed limitations are explicitly disclosed by Corio.

Regarding claim 19 Applicants respectfully resubmit the position regarding claims 14 and 15. It is further submitted that claim 19 contains further patentable subject matter not disclosed by Corio. Therefore, Applicants respectfully request reconsideration and withdrawal of the above-noted rejection.

Attached hereto is a marked-up version of the changes made to the Specification by the current amendment. The attached page is captioned: "Version with Markings to Show Changes Made."

This Application is believed to be in condition for allowance and such action at an early date is earnestly solicited. If the Examiner believes that a telephone interview may expedite the prosecution of the Application, the Examiner is invited to contact the below attorney at the indicated telephone number.

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Specification

In the FIG. 3, please include reference indicator 300 and amend the reference numerals for the video memory (formerly 322) coupled to the graphics adaptor 330 to "332" as indicated in the accompanying red-lined drawing.

In the Specification

In the Specification, in the "Background of the Invention" section, on page 1, please amend the second paragraph beginning at line 16 to read as follows:

The prior art configuration of Figure 1 can be inefficient because of the need to transport the video data across the PCI bus. In order for the decoded data to be stored within the graphics adapter's video memory, it is necessary for the video decoder to have its PCI bus control logic to store the rendered video information within the video memory. The hardware[necessarily of] <u>necessary for</u> the video decoder to interface to the PCI bus is costly in terms of space and design implementation. Another inefficiency of the system of Figure 1 is the use of PCI bandwidth by the video decoder when transmitting the data to the video memory. The video decoder is capable of performing the data transfer, and does not require system processor intervention. However, the system processor can be [stall]<u>stalled</u> if it needs to access the PCI bus during a transfer of video data by the video decoder. Therefore, the bandwidth used by the video decoder can prevent a system processor, or any other peripheral requiring the PCI bus, from functioning optimally when unable to access the PCI bus. For example, for a 320-by-240 pixel screen the number of bytes of data that [needed]<u>need</u> to be transferred each second between the video decoder and the video memory would be at least 320 x 240 x 2 bytes x 60 frames per second.

In the "Detailed Description of the Drawings" section, please amend the paragraphs beginning on page 4 at line 4 to read as follows:

The portion 300 may include discrete add-on cards in a general purpose computer, components integrated on a mother board, [such as]such as Application Specific Integrated circuits (ASICs) or data processors. This bus 340 may be any number of connectors, including ribbon cable connecting two separate add-on boards, a bus integrated onto a mother board, or connector pins associated with a bus where the video decoder actually plugs into the graphics adapter 340.

In operation, a video-in signal is received at the video decoder 310. The video-in signal can be representative of any number of video signals. For example, the video-in could be a compressed video signal such as an MPEG video signal, a DVD video signal, a video signal from a VCR, a television, or any other video source. The video decoder 310 converts the video-in to a video source signal usable by the graphics adapter 320. Once the video-in conversion process is completed by the decoder 310, the video source is transmitted across the dedicated local bus 340 to the graphics adapter 320. In other embodiments, the dedicated video bus 340 could be connected to other peripheral boards as well. However, in accordance with this specific embodiment, video data will not be transmitted across the system bus 350. The data transmitted across the bus 340 is captured into the video memory 322 by the graphics adapter 320. Once captured at the video memory 322, it is possible to retrieve the data from the video memory 322 and display it visually onto the monitor 324.

In the "Detailed Description of the Drawings" section, please amend the paragraph beginning on page 5 at line 11 as follows:

If the application window is moved to a different monitor, or a portion of the window is moved to a different monitor, such as monitor 334 associated with graphics adapter 330, the following sequence of events will occur. The operating system, in response to the user's inputs, would transmit operating system commands indicating the new window location. These operating system commands are interpreted by the graphics adapters 320 <u>and 330</u> at memory 322[and 330]. In response, the graphics adapter 330 will recognize that a portion of its video memory is to be displayed. However, all of the video data to be displayed is still being received and stored by the graphics adapter 320. Therefore, it is necessary for graphics adapter 320 to recognize the application window previously being displayed exclusively on monitor 324 is now at least partially being displayed on monitor 334. In response, the graphics adapter 320 will determine that portion of it video memory 322 that is now to be displayed by the adapter 330. This portion of the memory 322 will be sent to the adapter 330 using a transfer technique, such as a DMA transfer. DMA hardware capable of [transmitted]<u>transmitting</u> the video to the appropriate video memory location in video memory 332 can be located on VGA 320.

In the "Detailed Description of the Drawings" section, on page 8 beginning at line 4, please amend the following paragraphs to read as follows:

The I/O adapter is further connected to disk drives 447, printers 445, removable storage devices 446, and tape units (not shown) [to] via bus 402. Other storage devices may also be interface to the bus 412 through the I/O adapter 422.

A communication adapter 424 is connected to bridge 450 and/or modem 451. Furthermore, a video/graphic controller 426S connects the system bus 402 to a display device 460.

On page 9, beginning at line 8, please amend the following paragraphs to read as follows:

In operation, the bus 402 could correspond to the PCI bus 350 of FIG. 3, and the video graphics adapters would be connected to bus 402 in the same manner as controller 426. In addition, methods associated with the present invention, if any, may be implemented and stored on computer readable media such as one or more of the storage devices 445, 446, and [$47]447 for subsequent processing by CPU 410. Since the apparatus implementing the present invention is, for the most part, composed of electronic components and circuits known to those skilled in the art, circuit details will not be explained in any greater extent than that considered necessary as illustrated above, for the understanding and appreciation of the underlying concepts of the present invention and in order not to obfuscate or distract from the teachings of the present invention.

One method of recognizing the video decoder 310 on remote bus 340 is put forth in Patent Application having attorney docket number 9900300, entitled "Method and Apparatus for Configuring a Computer System, filed on [February, XX]March 19, 1999, and having Application Number [09/XXX,XXX (To be assigned)]09/272,464, owned by instant Assignee and is hereby incorporated by reference.

Next, in step 511, an application start-up occurs. In a [Specific]specific embodiment, the application is an active video application whereby an active video signal is received and displayed within a window opened by, or for, the application. For example, if a user

[chose]chooses to watch a television program on a computer screen, an application capable of displaying such a television program would be executed.

On page 10, beginning on line 7, please amend the following paragraph to read as follows:

Once the first video system recognizes that a portion of the window has moved to a monitor controlled by a different video controller, it will send the captured video to the second VGA. Generally, this would be accomplished across the system bus, such as the PCI bus. This is done generally by a direct memory access (DMA) type device that is controlled by the adapter that [monitoring]monitors systems calls, and is aware of the new location in the other adapter where to map the captured data. One of ordinary skill in the art will recognize that in other implementations, instead of having a DMA sending the captured data to the second video graphics adapters memory, it would be possible to intercept the data before it is stored in the first VGA's memory, thereby keeping just one copy at the location needed (the second VGA).

In the Claims:

Please amend Claims 3, 4 and 5 to read as follows:

1. (Once Amended) A method of displaying active video on a computer system, the method comprising the steps of:

receiving at a first video graphics adapter (VGA) a first frame of active video from a video source;

rendering at least a first portion of the first frame of video at the first VGA in response to a first control signal; and

rendering at least a second portion of the first frame of video at a second VGA in response to a second control signal.

3. The method of claim 1, wherein the step of rendering at least a first portion of the first frame of video at the first VGA includes storing the at least a first portion of the active [decoded]video in a video memory associated with the first VGA.

4. The method of claim 3, wherein the step of rendering at least a second portion of the first frame of video at the second VGA includes the substep of:

storing the at least second portion of the active [decoded]video in a first video memory associated with the first VGA.

5. The method of claim 4 further including the substep of:

reading the second portion of the active [decoded]video from the first video memory and storing the at least second portion of the active [decoded]video in a first video memory associated with the first VGA.

11. (Once Amended) The method of claim 1 further comprising the steps of:

receiving at the second VGA a second frame of active video from a second video source; <u>and</u>

rendering at least a portion of the second frame of video at the first VGA.

14. (Once Amended) A processing system for executing instructions, the processor system comprising instructions for: 536, 537, 538, 547

monitoring the location of an active video window;

storing active video data at first video memory; <u>and</u>

sending the active video data from the first memory to a second video memory when the location of the active video window is associated with the second video memory.

15. (Once Amended) A method of displaying active video on a computer system, the method comprising the steps of:

receiving at a first video graphics adapter (VGA) a first frame of active video from a video source<u>; and</u>

displaying at least a first portion of the first frame of video at a second VGA in response to a second control signal.